ANKIT KAUL

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Short bio: Ph.D. student in Electrical and Computer Engineering with a focus on 3D integration of compute in-memory (CIM) systems. Experience in: Device-package-application analysis of heterogeneous integration for CIM, 3D integration using hybrid bonding (SoIC), power/thermal management techniques, die-to-die interconnection evaluation, power delivery circuits, micro-architecture analysis.

EDUCATION

Georgia Institute of Technology, Atlanta, GA — **Ph.D., Electrical and Computer Engineering**, **GPA: 3.7** — *May 2018 – Jul. 2023 (expected)*
Minor: Computer Science

Georgia Institute of Technology, Atlanta, GA — **Master of Science, Electrical and Computer Engineering**, **GPA: 3.65**
Aug. 2016 – May 2018
Focus: Digital systems and Computer architecture

Key coursework (MS+Ph.D): IC Fabrication, Hardware acceleration for Machine Learning, Advanced Computer Architecture, Interconnection Networks (Network on Chip), Digital Systems at Nanometer Nodes, Advanced Digital Design with Verilog, Advanced VLSI Systems.

R.V. College of Engineering, Bangalore, India — **Bachelors, Electrical Engineering, GPA: 9.05/10.0** — *Aug. 2009 – May 2013*

EXPERIENCE

Graduate Research Assistant, Integrated 3D systems lab, (SRC ASCENT student) Georgia Institute of technology – Atlanta, GA
May 2018 – Present

- **Research focus**:
  - Impact of 3D integration on emerging non-volatile memory-based compute in-memory (CIM) inference accelerators
  - Die-to-die interconnection evaluation, power/thermal management techniques, novel power delivery techniques for 2.5D/3D
- **Adviser: Dr. Muhannad Bakir** (https://bakirlab.gatech.edu/)

Advanced Packaging Research Intern, AMD – Austin, TX — *Jan. 2022 – May. 2022*

- Computational modeling and pathfinding for 3D V-cache SoIC integration architectures and advanced materials for superior thermal and electrical performance (**Python, 3D partitioning**). **Advisers**: Hemanth Dhavaleswarapu, Rahul Agarwal

Ph.D. Intern - Advanced Products, Physical IP, Arm Inc. – Austin, TX — *May 2020 – Aug. 2020*
Project: Power-performance-thermal evaluation for 2.5D integration of arm-based 7nm high-performance systems

- Developed a methodology to explore relationship between core implementation targets, DVFS points, thermal limits, and system throughput for multi-die integration architectures. (**Python, Celsius, Tcl**) **Advisers:** Jim Dodrill, Saurabh Sinha
- **DAC 2022** poster titles: "Signaling and Thermal Considerations for 2.5D Integration of Arm-Based 7nm High-Performance Systems," journal publication in progress.

Impact: Improved Arm's 2.5D modeling methodology by developing multi-core SiP analyses capability for large-scale compute

UTC Aerospace Systems, Hardware Engineer – Bangalore, India — *Jul. 2013 – Jul. 2016*
Led platform circuit performance analysis of an Electronic Control and power quality Monitoring (ECM) unit for Boeing's 777x

Impact: Achieved **$50k savings** by improving circuit performance via analysis of tolerance bottlenecks using Allegro AMS Simulator

SELECTED PUBLICATIONS[#]

[#] >15 publications in heterogeneous integration/interconnection/device areas through conferences, journals, book chapters. Complete list: https://tinyurl.com/54tc9zbj
*****: Equal contribution

1. **A. Kaul**, X. Peng, S. K. Rajan, S. Yu and M. S. Bakir, "Thermal Modeling of 3D Polylithic Integration and Implications on BEOL RRAM Performance," *IEEE International Electron Devices Meeting (**IEDM**)*, 2020, pp. 13.1.1-13.1.4, doi: 10.1109/IEDM13553.2020.9371983.
2. X. Peng, **A. Kaul**, M. S. Bakir, and S. Yu, "Heterogeneous 3D Integration of Multi-Tier Compute-in-Memory Accelerators: An Electrical-Thermal Co-Design," *IEEE Transactions on Electron Devices (**TED**)*, Sep. 2021 doi: 10.1109/TED.2021.3111857.
3. Y. Luo, S. Dutta, **A. Kaul**, S. Lim, M. Bakir, S. Datta, S. Yu, "Monolithic 3D Compute-in-Memory Accelerator with BEOL Transistor based Reconfigurable Interconnect," *IEEE International Electron Devices Meeting (**IEDM**)*, 2021, pp. 25.3.1-25.3.4.
4. X. Peng, W. Chakraborty, **A. Kaul**, W. Shim, M. S. Bakir, S. Datta, S. Yu, "Benchmarking Monolithic 3D Integration for Compute-in-Memory Accelerators: Overcoming ADC Bottlenecks and Maintaining Scalability to 7nm or Beyond," *IEEE International Electron Devices Meeting (**IEDM**)*, San Francisco, CA, Dec. 2020.
5. **A. Kaul**, S. K. Rajan, M. O. Hossen, G. S. May, and M. S. Bakir, "BEOL-Embedded 3D Polylithic Integration: Thermal and Interconnection Considerations," *IEEE Electronic Components and Technology Conf. (**ECTC**)*, Orlando, FL, May 2020 *(**Nominated for EPS/ECTC Student Travel Award: Top 22 out of 71 student submissions**)*.
6. T. Zheng*, **A. Kaul***, S. Kochupurackal Rajan*, and M. S. Bakir, "Polylithic Integrated Circuits using 2.5D and 3D Heterogeneous Integration: Electrical and Thermal Design Considerations and Demonstrations," in B. Keser, and S. Kröhnert (Ed.), *Embedded and Fan-Out Wafer and Panel Level Packaging Technologies for Advanced Application Spaces* (pp. 261-287) ***Wiley***, 2021.
7. R. Saligram, **A. Kaul**, M. S Bakir and A. Raychowdhury, "A Model Study of Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication in 2.5D Integration," *IFIP/IEEE Inter. Conf. on Very Large Scale Integration (**VLSI-SoC**)*, Salt Lake City, UT, Oct. 2020.

8. M. O. Hossen, **A. Kaul**, I. Ganusov, E. Nurvitadhi, M. Pant, R. Gutala, A. Dasu, and M. S. Bakir, "Modeling of Power Delivery Network (PDN) in Bridge-Chips for 2.5-D Heterogeneous Integration Technologies," in *IEEE Transactions on Components, Packaging and Manufacturing Technology (**TCPMT**), 2021 (to appear)*.
9. **A. Kaul**, Y. Luo, X. Peng, S. Yu and M. S. Bakir, "3D Heterogeneous Integration of RRAM-Based Compute-In-Memory: Impact of Integration Parameters on Inference Accuracy." *(under review)*
10. L. Zhu, T. Ta, R. Liu, R. Mathur, X. Xu, S. Das, **A. Kaul**, A. Rico, D. Joseph, B. Cline, S. K. Lim, "Power Delivery and Thermal-Aware Arm-Based Multi-Tier 3D Architecture," *IEEE/ACM Inter. Symp. on Low Power Elec. and Design (**ISLPED**)*, 2021.

TECHNOLOGY SUMMARY

Languages: Python, Matlab, Verilog HDL, C++, shell, D3.js

EDA tools: HSPICE, Cadence Celsius, Cadence Virtuoso, ANSYS Mechanical and Fluent, Synopsys VCS, Calibre, Allegro PCB

Skills: 3D Integration, SoIC design and process flow, hybrid bonding, microelectronic packaging, 3DIC partitioning and non-volatile memory/logic integration, electrical modeling and evaluation of die-to-die signaling metrics, thermal and power delivery modeling for heterogeneous integration, TSV and I/O HSPICE modeling, analytical multi-physics device-system analyses, vector-based power and thermal analysis for multi-core SiPs, computer architecture, unix, data analytics and visualization

AWARDS AND RECOGNITION

- Awarded the **J.N. Tata Endowment**: Scholarship for graduate research, selected among top 40 from 1000+ applicants, 2016-18.
- Nominated for the **Colonel Oscar P. Cleaver Award** for most outstanding Ph.D. dissertation proposal, Georgia Tech. ECE, 2021.
- Nominated for the **EPS/ECTC Conference Student Travel Award**: Top 22 out of 71 student research papers, 2020.

ACADEMIC PROJECTS

Study of limits on accelerator performance due to DRAM performance degradation – individual contributor *Jan. 2019 – May 2019*

Characterized temperature-driven bandwidth loss in DRAMs and studied the impact of this loss on the runtime performance of systolic CNN hardware accelerator configurations (evaluation tool: **SCALE-SIM systolic CNN accelerator simulator**)

- Established that ~12% temperature-driven DRAM BW loss can lead to ~50% increase in runtime for considered MLPerf DNN workloads

(**Report**: https://www.dropbox.com/s/jprs23jbmr3kh9c/Kaul_ece8893_final_report.pdf?dl=0)

Achieving High-Radix Topology Performance using SMART Networks – individual contributor *Jan. 2018 – May 2018*

Proposed a design with multiple SMART (Single-Cycle Multihop Asynchronous Repeated Traversal) Network-on-Chip (NoC) mesh networks in parallel to achieve saturation throughput comparable to high-radix topologies (evaluation tool: **Garnet 2.0 NoC architecture simulator**)

- Demonstrated higher theoretical throughput of a SMART mesh over fbfly variants for heterogeneous traffic with 64 routers

(**Report**: https://www.dropbox.com/s/v5bvtq33uehfn3s/CS8803-Report_Kaul.pdf?dl=0)

Systolic array RTL implementation, simulation and synthesis for CNN accelerators – individual contributor *Feb. – Mar. 2019*

Implemented (**Verilog**) a systolic array of processing elements (PE) to demonstrate matrix multiplication using output stationary dataflow

- Performed functional verification (**DVE**) and estimated area and power (**Design Compiler**) (course: H/W for ML)
- Synthesized design using Nangate 15nm targeting 1GHz, and reported 9.217 mW at an area of 11809 um^2 for an 8x8 array of PEs

PROFESSIONAL ACTIVITIES AND SERVICE

A. Professional Contribution:
   - Technical Journal Referee: IEEE Transactions on Electron Devices (TED), IEEE Electron Devices Letters (EDL), IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021-2022

B. Membership:
   - Graduate Student Member: IEEE, Electron Devices Society (EDS), Electronics Packaging Society (EPS)

C. Mentorship:
   - Biya Haile, previously BS AE/ECE, current Ph.D. student, ECE, Georgia Tech., bhaile3@gatech.edu.